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# REAL TIME IMPLEMENTATION AND VERIFICATION OF EBERS-MOLL MODEL

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## ABSTRACT

Today's in any electronic circuit diode and transistor are essential components. It is too much difficult to design or implement a circuit without these two silicon made devices. From the point of fabrication and atomic structure, diode is single junction component whereas transistor is double junction. As per this simple construction a normal though can arise from any human mind, why a transistor cannot make by simply connecting two diodes? The answer for this question is very well explained by Ebers Moll model in theoretical way. By this article we have tried to demonstrate the same concept practically. By performing various experiments like i/p-o/p characteristics, DC-AC analysis, etc. for both, one is single transistor and later one is two back to back diode combinations, it is easy to answer mentioned question.

**KEYWORDS:** Ebers Moll Model, Diode 1N4007, Transistor BC547, Saturation Condition

## INTRODUCTION

In Figure 1 we see the Ebers Moll model for p–n-p transistor. It involves two ideal diodes placed back to back with reverse saturation current $-I_{EO}$ and $-I_{CO}$ and two dependent current controlled sources shunting the ideal diodes.

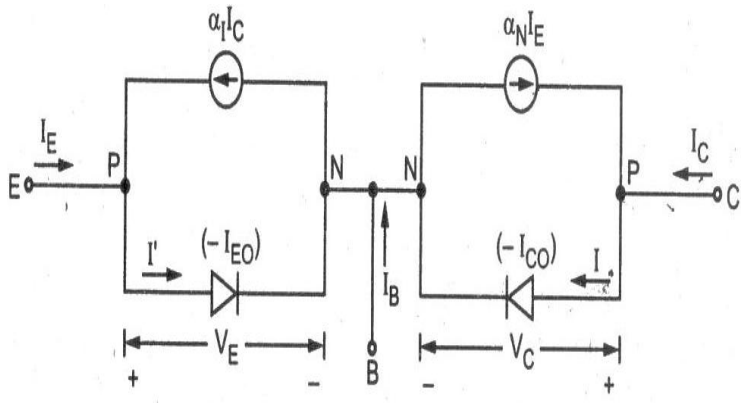


**Figure 1: The Ebers-Moll Model for PNP Transistor**

Let us see the equations of Ic and IE from Ebers – moll model. Applying KCL to the collector node, we get

$$\alpha_N I_E + I_C = 1$$

$$I_C = I - \alpha_N I_E$$
$$I_C = -\alpha_N I_E + I_O(\mathrm{eV}_C / \mathrm{V}_T - 1)$$
$$\mathrm{I}_O = -I_{CO}$$
$$I_C = -\alpha_N I_E - I_{CO}(\mathrm{eV}_C / \mathrm{V}_T)$$

The general expression for collector current IC of a transistor for any voltage across collector junction Vc and emitter current IE is

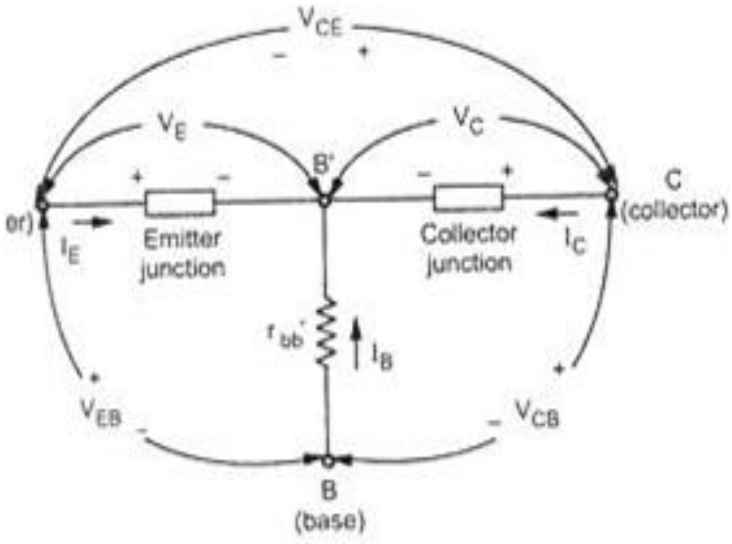


**Figure 2: The Ebers-Moll Model for PNP Transistor**

$$I_C = -\alpha_N I_N + I_{CO}(\mathrm{eV}_C / \mathrm{V}_T - 1)$$

Here, subscript N to α indicates that we are using transistor in a normal manner. When we interchange the role of emitter and collector we operate transistor in a inverted function. In such case current and junction voltage relationship for transistor is given by

$$I_E = -\alpha_I I_C - I_{EO}(\mathrm{eV}_E / \mathrm{V}_T - 1)$$

Here, subscript I to α indicates that we are using transistor in a inverted manner, αI is the inverted common – base current Gain.

IEO – The emitter junction reverse saturation current.

VE – The voltage drop from p – side to N – side at the emitter junction.

Similarly applying KCL to emitter node we get

$$I_E + \alpha_I I_C = I$$
$$I_E = I - \alpha_I I_C$$
$$I_E = -\alpha_I I_C + \mathrm{I}_O(\mathrm{eV}_E / \mathrm{V}_T - 1)$$
$$I_C = -\alpha_I I_C - I_{EO}(\mathrm{eV}_C / \mathrm{V}_T)$$

This model is valid for both forward & reverse static voltages applied across the transistor junction. In the above model, by making the base width much large than the diffusion length of minority carriers in the base, all mining carriers will recombine in the base and none will survive to reach the collector [1].

## IMPLEMENTATION

For this research paper two different circuits have been implemented practically on the bread board, one is for transistor and second is for back to back diodes. During implementation Transistor BC547 (NPN) and diode (1N4007) has been used. Initially we have started with DC analysis and then AC analysis also carried out.

In table 1 the dc analysis of transistor has been shown. We have shown i/p and o/p characteristics. During analysis the saturation point has been highlighted.

**Table 1: Transistor Characteristics Analysis at Vcc=5V**

| Vbb (Volts) | I/P Characteristics Vbe (Volts) | Ib(mA) | O/P Characteristics Vce (Volts) | Ic(mA) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0.76 | 1.349 | 0.02 | 4.8 |
| 2 | 0.82 | 7.3 | 0.02 | 4.8 |
| 3 | 0.84 | 14.2 | 0.03 | 4.8 |
| 4 | 0.87 | 22.1 | 0.03 | 4.8 |
| 5 | 0.88 | 28.9 | 0.04 | 4.8 |
| 6 | 0.90 | 38.5 | 0.04 | 4.8 |

**Table 2: Diode Characteristics Analysis at Vcc=5V**

| Vbb (Volts) | I/P Characteristics Vbe (Volts) | Ib(mA) | O/P Characteristics Vce (Volts) | Ic(mA) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0.61 | 2.7 | 4.98 | 0 |
| 2 | 0.66 | 8.7 | 4.98 | 0 |
| 3 | 0.70 | 17.3 | 4.98 | 0 |
| 4 | 0.72 | 28.2 | 4.98 | 0 |
| 5 | 0.73 | 36.2 | 4.98 | 0 |
| 6 | 0.74 | 46 | 4.98 | 0 |

**Table 3: Diode Characteristics Analysis at Vcc=5V**

| Vbb (Volts) | I/P Characteristics Vbe (Volts) | Ib(mA) | O/P Characteristics Vce (Volts) | Ic(mA) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0.27 | 4.8 | -0.07 | 4.7 |
| 2 | 0.63 | 9.4 | -0.11 | 4.9 |
| 3 | 0.68 | 17.5 | -0.13 | 4.9 |
| 4 | 0.71 | 26.8 | -0.15 | 4.9 |
| 5 | 0.72 | 36.4 | -0.16 | 4.9 |
| 6 | 0.73 | 46 | -0.18 | 4.9 |

In table no.2 two back to back diode circuit analysis carried out with vcc=5v and vcc=-5v. in figure 1 we have compare the characteristics graphically.

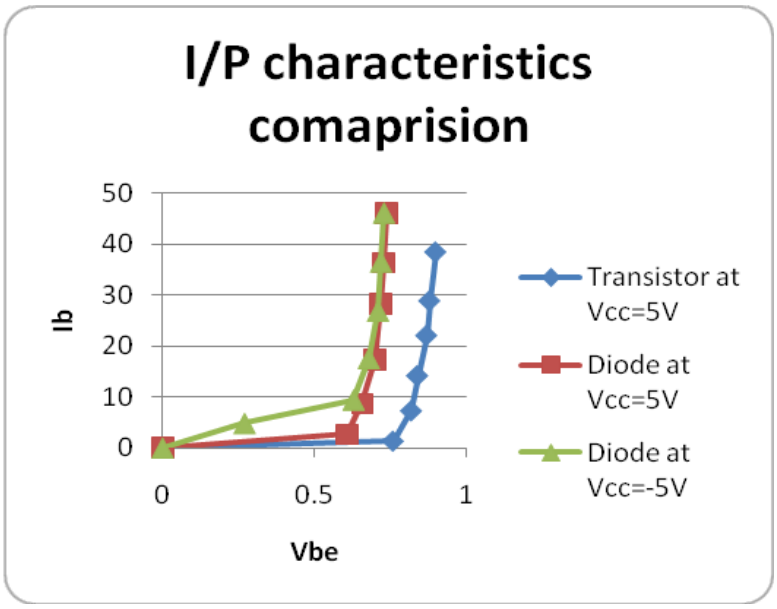


**Figure 3: Input Characteristics Comparison for Transistor and Back to Back Diode**

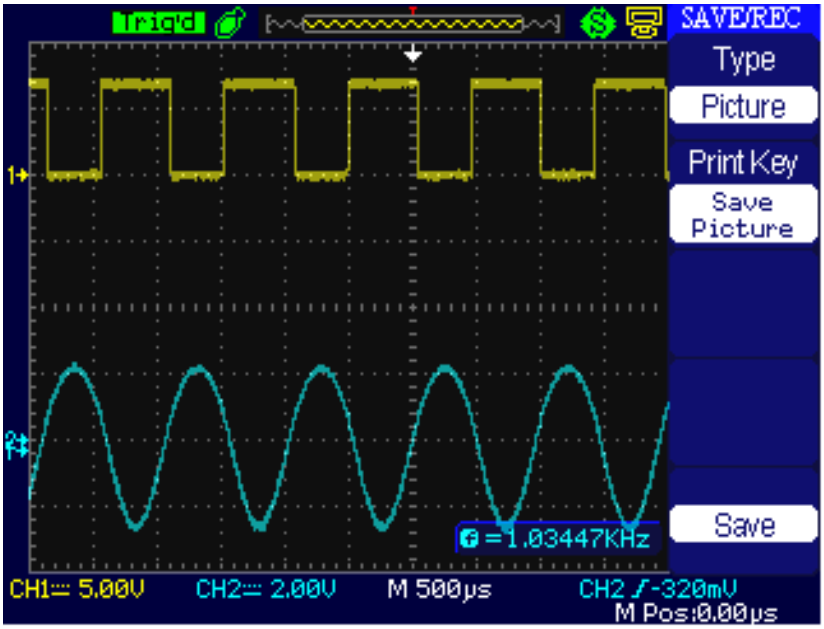


**Figure 4: DSO O/P for Back to Back Diode Case Input Character**

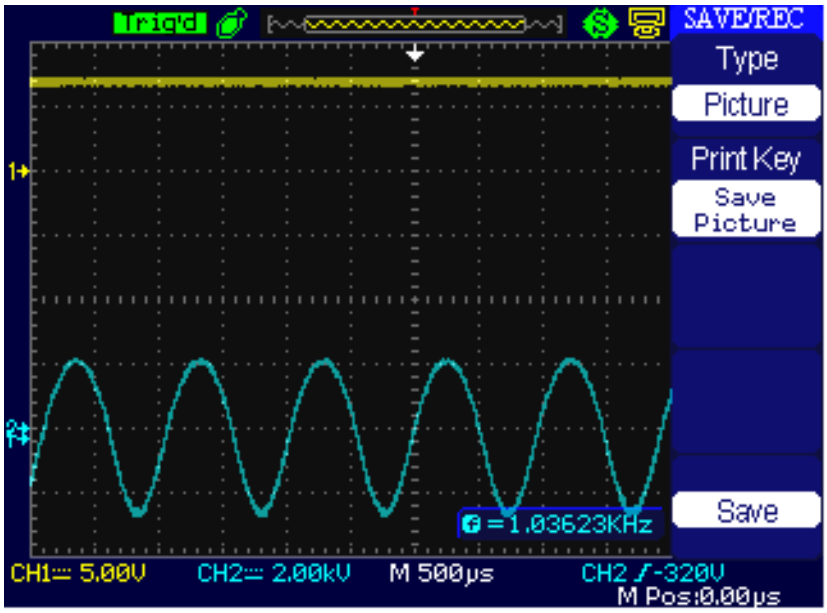


**Figure 5: DSO O/P for Transistor Case**

In Figure 4 and Figure 5 AC analysis has been shown by using DSO 5025-A. In figure 4 it has been clearly shown that we are getting phase shift in transistor case but in Figure 5 we are not getting any type of result in back to back diode scenario.

## CONCLUSIONS

As per the Ebers moll mode condition, transistor action ceases, and we simply have two diodes placed back to back diodes. The result of DC analysis clearly indicates th difference between characteristics of a transistor and back to back diodes combination. Not only in the DC analysis but by observing waveform result for AC analysis we can differentiate both the cases. Therefore it is impossible to construct a transistor by simply connecting two separate diodes back to back. Simply,

Transistor ≠ Diode + Diode

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